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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,594	04/08/2004	Yen-Fu Chiang	BCS03206	8117

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GENERAL INSTRUMENT CORPORATION DBA THE CONNECTED
HOME SOLUTIONS BUSINESS OF MOTOROLA, INC.
101 TOURNAMENT DRIVE
HORSHAM, PA 19044

EXAMINER	
JACKSON, BLANE J	
ART UNIT	**PAPER NUMBER**
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,594	CHIANG ET AL.	
	Examiner	Art Unit	
	Blane J. Jackson	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,7 and 10-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7 and 10-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's Amendment with arguments, see the applicant's Remarks filed 13 November 2006, with respect to the rejection(s) of claim(s) 1-5, 6, 7, 10-18, 20 and 21 under Kawakami et al. have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is based on Kawakami et al. in view of Fessler et al. (US 7,016,198).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, 7, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami et al. (US 2005/0122428) in view of Fessler et al. (US 7,016,198).

As to claim 1, Kawakami teaches a radio frequency (RF) tuner comprising:

A tuner housing (figure 13, paragraph 0076, tuner (81), one of two shown mounted parallel to each other, comprising an EMI shielding structure including the walls, cover (212) and the ground plane (81B)),

A cover coupled to a first side of said housing (figure 13, paragraph 0076, tuner (81) with shield plate (212)),

A tuner printed circuit board (PCB) coupled to a coupled to a second side of said housing wherein the PCB comprises a component connection layer and a second ground layer that does not have any signal path circuitry, the *second layer* is configured to shield the tuner PCB (figures 12A and 13, paragraphs 0068-0069, a double sided printed circuit board (21) comprises components mounted to the wiring side layer (81A) and the opposite board surface includes an overall conductive pattern or ground plane (81B) to act as an EMI shield which is connected to a ground pattern of the component side surface and a frame-like or component wall shield plate (212)).

Kawakami further discloses an embodiment of a three layer PCB shown in figure 10, paragraphs 0058-0061, the PCB includes a component mount layer (13), a first ground layer (15) and a second ground layer (17) but does not teach a four layer PCB comprising a component connection layer, a first ground layer for a first set of signal path circuitry, a second ground layer for a second set of signal path circuitry and a third ground layer that does not have any signal path circuitry.

Fessler teaches several embodiments of a multi-layer printed circuit board where the outer layers are configured to reduce electromagnetic emissions from the PCB, column 5, line 5 to column 2, line 62. Fessler discloses a well known configuration for multilayer PCB comprises all signal traces on internal conductive layers and locate dedicated ground planes on the outer two PCB layers, the components mounted to the

top outer layer and electrically connected to the bottom outer layer that forms as large and contiguous ground plane area as possible, column 1, line 63 to column 2, line 16.

Since Kawakami teaches the application of a double or three layer printed circuit boards, figures 10 and 13, it would have been obvious to one of ordinary skill in the art at the time of the invention to configure the multi-layer PCB of Kawakami in accordance to the multi-layer approach of Fessler to shield high frequency signal traces placed on internal conductive layers with outer ground plane layers to reduce electromagnetic emission from the PCB.

As to claim 6, Kawakami teaches the RF tuner of claim 1 further comprising a network connector communicatively coupled to said tuner PCB (figures 12A and 13, paragraphs 0070 and 0076, connector (218)).

As to claim 7, Kawakami teaches the RF tuner of claim 6, wherein said network connector comprises a coaxial cable connector (paragraph 0070, antenna input coaxial RF connector (218)).

As to claim 14, Kawakami teaches a set-top box comprising:

A chassis (figure 9, paragraphs 0059-0061, set-top box (30)),

A tuner coupled to said chassis (figure 9, paragraph 0059tuner circuits 1 and 2 arranged parallel to each other),

A demodulator communicatively coupled to said tuner (figure 9, paragraph 0060, Demux (31)) and

A central processing unit (CPU) communicatively coupled to said demodulator (figure 9, paragraph 0060, CPU (34)),

Wherein said tuner includes a tuner housing, a cover coupled to a first side of said housing and a tuner printed circuit board (PCB) including a plurality of layers coupled to a second side of said housing wherein said layers are configured to shield said tuner PCB (figures 12A and 13, paragraphs 0068-0076, EMI shield structure of tuner (81) comprising ground surface (81B) of double sided printed board (210), figure 3, paragraph 0016; frame-like walls (94) and shield plates (212)).

Kawakami further discloses an embodiment of a three layer PCB shown in figure 10, paragraphs 0058-0061, the PCB includes a component mount layer (13), a first ground layer (15) and a second ground layer (17) but does not teach a four layer PCB comprising a component connection layer, a first ground layer for a first set of signal path circuitry, a second ground layer for a second set of signal path circuitry and a third ground layer that does not have any signal path circuitry.

Fessler teaches several embodiments of a multi-layer printed circuit board where the outer layers are configured to reduce electromagnetic emissions from the PCB, column 5, line 5 to column 2, line 62. Fessler discloses a well known configuration for multilayer PCB comprises all signal traces on internal conductive layers and locate dedicated ground planes on the outer two PCB layers, the components mounted to the

top outer layer and electrically connected to the bottom outer layer that forms as large and contiguous ground plane area as possible, column 1, line 63 to column 2, line 16.

Since Kawakami teaches the application of a double or three layer printed circuit boards, figures 10 and 13, it would have been obvious to one of ordinary skill in the art at the time of the invention to configure the multi-layer PCB of Kawakami in accordance to the multi-layer approach of Fessler to shield high frequency signal traces placed on internal conductive layers with outer ground plane layers to reduce electromagnetic emission from the PCB.

As to claim 17, Kawakami teaches the set-top box of claim 14 wherein said tuner further comprises a vertical mount tuner (figure 13, paragraph 0073, two tuners (81) and (82) are shown and described as mounted to the main board, the ground surfaces (81B) and (82)B are parallel to each other and an RF connector of each tuner projects through a rear end panel (301) of the set-top box).

Claims 2, 3, 11, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami et al. (US 2005/0122428) and Fessler (US 7,016,198) in view of Yi et al. (US 2005/0042928).

As to claims 2, 11 and 15 with respect to claims 1, 8 and 14, Kawakami of Kawakami modified teaches the RF tuner of claim 1 wherein the tuner PCB further comprises a plurality of *finger connector pins* (figure 12A, pins (219) formed in the tuner PCB layers to electrically couple the tuner PCB to a second PCB, paragraph 0074.

Kawakami modified does not teach a plurality of *finger connector extrusions* formed in the tuner PCB to electrically couple the tuner PCB to a second PCB.

Yi teaches a printed circuit card edge connector (1) which electrically couples a daughter PCB (6) with finger connector extrusions to a second or mother PCB (5), figure 1, paragraphs 0004-0008.

It would have been obvious to one of ordinary skill in the art to modify the signal pins of Kawakami modified with the PCB edge connector approach of Yi for simple and reliable connection of two printed circuit cards.

As to claim 3, Kawakami teaches the RF tuner of claim 2 wherein said tuner further comprises a vertical mount tuner (figure 13, figure 4, prior art and figure 13, paragraphs 0006, 0073, two tuners are taught mounted to the rear wall and coupled vertically to the main set-top box PCB).

As to claim 12, Kawakami teaches the RF tuner of claim 11 wherein said second PCB comprises a main PCB of a set-top box (figure 9, paragraphs 0059-0061, set-top box (30)).

As to claim 16, Kawakami teaches the set-top box of claim 15 wherein said second PCB comprises a main PCB of said set-top box (figure 13, paragraph 0073, tuner (81) is mounted to the main printed board (302)).

Claims 4, 10, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami et al. (US 2005/0122428) and Fessler et al. (US 7,016,198) in view of Donaldson (US 4,370,515).

As to claims 4 and 18, Kawakami teaches the RF tuner of claim 1 and the set-top box of claim 14 wherein said tuner housing further comprises a plurality of support members (figures 3 and 12A, frame like shield plates (94) although discussed for the prior art is seen as applicable in figure 12A and 13) and a shield cover, figure 13, shield plate (212), paragraph 0076, but is silent as to a plurality of extrusions, said extrusions being configured to extrude through a plurality of corresponding orifices or plated through holes in said tuner PCB or a plurality of ribs configured to receive a corresponding plurality of clip tabs of the cover.

Donaldson teaches a shielding structure (102) having peripheral walls of sheet metal with tabs (106) extending into apertures of a printed circuit board (108), figures 10 and 11, column 5, line 34 to column 6, line 4. Donaldson also teaches a plurality of ribs configured to receive a corresponding plurality of clip tabs or spring clips of the cover, column 5, lines 54-66.

Since Kawakami teaches a plurality of support members and shield cover, it would have been obvious to one of ordinary skill in the art at the time of the invention to identify the attachment of the shield walls and cover to the PCB of Kawakami in the method of Donaldson to provide an inexpensive and electrically tight solution (Donaldson-column 1, line 50 to column 2, line 12) for bonding together the shield structure.

As to claims 10 and 20, Donaldson of Kawakami modified teaches the RF tuner of claim 1 and the set-top box of claim 18 further comprising a plurality of plated through holes disposed through the PCB layers (figure 10, column 5, lines 34-54, tabs (94) along the walls (90) for insertion into apertures (96) of the printed circuit board (86) and coupled to the PCB mechanically and electrically by wave soldering to the top layer ground traces and plated through holes).

Claims 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami et al. (US 2005/0122428) and Fessler et al. (US 7,016,198) in view of Nishimura et al. (US 6,522,872).

As to claims 13 and 21, Kawakami teaches the RF tuner of claim 8 and the set-top box of claim 19 wherein said tuner components comprise a down converter VCO, figure 6, paragraphs 0054-0055 and 0059. Kawakami is silent as to an up-converter variable crystal oscillator.

Nishimura teaches a tuner circuit on a PCB within an EMI structure where the upconverter section and a down converter section are contained in separate respective shield portions of the tuner EMI structure, figures 1-3. Nishimura further teaches the upconverter (10) comprises a mixing circuit and a first PLL (111) and a first local oscillator (LO-1) and the down converter (20) includes a second PLL (21), a second local oscillator circuit (LO-2) and a down converter mixing circuit (D-MIX), column 4, lines 5-25.

Since Nishimura further teaches, with respect to claims 8 and 19, the signal line of the IF section is provided on an internal layer of a multilayered substrate and the signal line is surrounded with grounded conductive material on the upper a lower layers as a shield to noise (column 9, lines 24-28, it would have been obvious to one of ordinary skill in the art at the time of the invention to realize in the RF circuits of Kawakami the EMI structure of Kishimura such that multiple conversion circuits are contained in separate chassis for noise suppression.

Conclusion

The prior art made of record and not relied upon but considered pertinent to applicant's disclosure includes: Sun et al. (US 6,700,076).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J. Jackson whose telephone number is (571) 272-7890. The examiner can normally be reached on Monday through Friday, 8:30 AM-6:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BJJ